CLAIMS

We Claim:

1. An integrated circuit (IC) comprising:

programmable circuitry having programmable functions and programmable interconnections, the programmable circuitry comprising a first transmit port having a first fixed data width or a first variable data width, and a first receive port having a second fixed data width or a second variable data width;

a transceiver comprising a second transmit port having a third fixed data width or a third variable data width, and a second receive port having a fourth fixed data width or a fourth variable data width; and

a transmit converter coupling the first transmit port of the programmable circuitry and the second receive port of the transceiver, the transmit converter operably configured to convert the first fixed data width to the fourth variable data width, the first variable data width to the fourth fixed data width, or the first variable data width to the fourth variable data width.

2. The IC of Claim 1 further comprising,

a receive converter coupling the first receive port of the programmable circuitry and the second transmit port of the transceiver.

3. The IC of Claim 2, wherein the receive converter is operably configured to convert the third fixed data width to the second variable data width, the third variable data width to the second fixed data width, or the third variable data width to the second variable data width.

4. The IC of Claim 3, wherein a particular variable data width port has a data width that is a multiple of a data width of another particular variable data width port or a

particular fixed data width port, or a specific fixed data width port has a data width that is a multiple of a data width of a specific variable data width port.

5. The IC of Claim 3, wherein the receive converter comprises:

a first set of registers coupled to receive data of width N from the second transmit port of the transceiver, wherein the first set of registers is clocked by a first clock signal having a frequency f1, wherein N is an integer; and

a set of multiplexers coupled to the first set of registers, wherein the set of multiplexers is coupled to the first receive port of the programmable circuitry.

6. The IC of Claim 5, further comprising a second set of registers coupled to the set of multiplexers for receiving data of data width M, wherein the second set of registers is clocked by a second clock signal having a frequency f2, and wherein M is an integer.

7. The IC of Claim 1, wherein the transmit converter comprises:

a first set of registers coupled to receive data of width N from the first transmit port of the programmable circuitry, wherein the first set of registers is clocked by a first clock signal having a frequency f1, wherein N is an integer; and

a set of multiplexers coupled to the first set of registers, wherein the set of multiplexers is coupled to the second receive port of the transceiver.

8. The IC of Claim 7, further comprising a second set of registers coupled to the set of multiplexers for receiving data of data width M, wherein the second set of registers is

clocked by a second clock signal having a frequency f2, and wherein M is an integer.

9. An integrated circuit (IC) comprising programmable circuitry having programmable functions and programmable interconnections, the IC further comprising:

a first module having an output with a first variable data width;

a second module having an input with a fixed data width or a second variable data width; and

a data width converter receiving data from the output of the first module and sending the data to the input of the second module, the data width converter configured to convert data from the first variable data width to the fixed data width or the second variable data width.

10. The IC of claim 9 wherein the first module comprises circuitry selected from a group consisting of a serdes circuit, a transceiver, an I/O block, a microprocessor, and a configurable logic block (CLB).

11. An integrated circuit (IC) comprising programmable circuitry having programmable functions and programmable interconnections, the IC further comprising:

a first module having an output with a fixed data width;

a second module having an input with a variable data width; and

a data width converter receiving data from the output of the first module and sending the data to the input of the second module, the data width converter configured to convert data from the fixed data width to the variable data width.

12. An integrated circuit (IC) comprising:

a deserializer circuit for converting data from a serial format to a parallel format;

a data bus having a fixed data path width coupled to the deserializer circuit;

a variable width interface coupled to the data bus, the variable width receiver interface configured to convert data having the fixed data path width to data having a selectable data path width; and

a circuit having programmable functions and programmable interconnections, the circuit receiving the data having the selectable data path width.

13. The IC of Claim 12, wherein selectable data path width is selected from a group consisting of 1N, 2N, 4N, and 8N, wherein N is a positive integer.

14. A device comprising:

a circuit having programmable functions coupled to a variable data width interface by programmable interconnections, the programmable interconnections forming a first data path having a first variable data width selectable from a plurality of data widths, wherein the variable data width interface converts the first data path to a second data path, the second data path having a fixed data width or a second variable data width; and

a serializer circuit configured to transform data from a parallel format to a serial format, the serializer circuit coupled to the second data path.

15. The device of claim 14 further comprising:

a transmit processing block interposed between the variable width interface and the serializer circuit, the transmit processing block receiving data from the second data path and sending the data via a third data path having another fixed data width.

16. The device of claim 14 wherein the second data path has programmable interconnections.